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Lisa K. Jorgenson, Esq.
STMicroelectronics, Inc.
1310 Electronics Drive
Carrollton, TX 75006

EXAMINER	
CHOI, WOO H	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/943,242
Filing Date: August 30, 2001
Appellant(s): LIN, WEN

Kent A. Lemke
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 08, 2006 appealing from the Office action mailed February 10, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The Examiner does not agree with Applicant's characterization of prior art bus controllers as not being "operable to conduct mass storage transactions between the data or system memory and the mass storage devices without an intermediary mass storage controller" (see brief, pages 3-4). Applicant's bus controller is not disclosed to have any special feature, that is especially adapted to conduct mass storage transactions without an intermediary mass storage controller, that other prior art bus controllers do not have. The function of a bus controller is to

control access to the bus. A bus is simply a conduit through which data transfers can take place between devices attached to the bus. Any bus controller that controls access to the bus connecting the system memory with a mass storage device "without an intermediary mass storage controller" is **operable** to conduct such mass storage transactions. The basis for Applicant's claim to this limitation is the fact that Applicant calls the combination of a disk controller (figure 3, 303, see also paragraph 35) and a disk drive (figure 3, 307) a "mass storage device" and that there is no other mass storage controller between the "mass storage device" and the bus. Thus, this "feature" of the claimed bus being "operable to conduct ... without an intermediary mass storage controller" is not an actual novel feature of the bus controller, but it's a "feature" created by simply redrawing a functional box around a disk controller and a disk mechanism and calling that box a mass storage device that presumably does not require an intermediate mass storage controller.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US Patent Application Pub. No. 2003/0037198	Hunsaker
US Patent No. 6,601,126	Moriarty et al.

US Patent Application Pub. No. 2002/0144121 Ellison et al.

US Patent No. 6,493,656 Houston

Operating System: Design and Implementation, 1987, Prentice Hall, pages 92,114,118, 482-485 Tanenbaum

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 1 – 3, 5 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Hunsaker (US Patent Application Pub. No. 2003/0036198).

With respect to claim 1, Hunsaker discloses a computing system (figure 1) comprising:

a processor having a data/control bus interface (processor 110);

a data/control bus (host bus 120) implementing one or more device communication channels;

a mass storage device (170) having an interface for communicating mass storage transactions; and

a data memory (system memory 140, alternatively 130 + 140) coupled to and shared by both the processor and the mass storage device (the system memory is shared by the processor via the host bus 120, peripherals via primary bus 195 and other I/O devices including mass storage devices via the ICH 150);

a bus controller (ICH 150) having a memory interface coupled (150 is coupled to 140 via 130) to the data memory and a mass storage interface coupled to the mass storage device's

interface without an intermediary mass storage controller (150 is coupled directly to 170 without anything in between) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

2. Claims 1, 12 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Zaidi *et al.* (US Patent No. 6,601,126, hereinafter "Zaidi").

With respect to claim 1, Zaidi discloses a computing system (figure 28) comprising:

a processor having a data/control bus interface(CPU or CPU + cache);

a data/control bus (CPU bus or the bus connecting the cache to the bridge) implementing one or more device communication channels;

a mass storage device (DMA peripheral, see col. 27, lines 41 – 45) having an interface for communicating mass storage transactions; and

a data memory (DRAM) coupled to and shared by both the processor and the mass storage device (neither the CPU nor the DMA peripherals have exclusive access to the DRAM memory, the DRAM is shared by all components that has access to it);

a bus controller (bridge and MAC) having a memory interface coupled to the data memory (MAC is coupled to DRAM) and a mass storage interface coupled to the mass storage device's interface without an intermediary mass storage controller (bridge is coupled to DMA peripherals via a PCI bus without an intermediary controller) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access

to memory locations within the data memory between the data/control bus and the mass storage device.

3. Claims 1, 14 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriarty *et al.* (US Patent No. 6,128,669, hereinafter "Moriarty").

With respect to claims 1 and 14, Moriarty discloses a computing system (figure 1) comprising:

a processor having a data/control bus interface (100);

a data/control bus (102) implementing one or more device communication channels;

a mass storage device (118 and 144) having an interface for communicating mass storage transactions;

a data memory (104, or alternatively 112) coupled to and shared by the processor and the mass storage device; and

a bus controller (106, or alternatively 106 and 108) having a memory interface coupled to the data memory (106 is coupled to 104) and a mass storage interface coupled to the mass storage device's interface without an intermediary mass storage controller (106 is coupled to 120, note that there's no patentable distinction between Applicant's mass storage device, figure 3, 303 + 307, and Moriarty's mass storage device, 120 + 144, they both consist of a controller and a disk) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

4. Claims 1 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ellison *et al.* (US Patent Application Pub. No. 2002/0144121, hereinafter "Ellison").

Ellison discloses a computing system (figure 1C) comprising:

a processor having a data/control bus interface (processor 110);

a data/control bus (host bus 120) implementing one or more device communication channels;

a mass storage device (170) having an interface for communicating mass storage transactions;

a data memory (system memory 140 or alternatively 130 + 140) coupled to and shared by the processor and the mass storage device; and

a bus controller (ICH 150) having a memory interface coupled to the data memory (150 is coupled to 140 via 130) and a mass storage interface coupled to the mass storage device's interface without an intermediary mass storage controller (150 is directly coupled to 170 without anything in between) and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

The computing system comprises a set-top box including processes for implementing audio/video behaviors in the processor (page 1, paragraph 13).

5. Claims 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Houston *et al.* (US Patent No. 6,493,656, hereinafter "Houston").

Houston discloses a computing system (figure 1) comprising:

a processor (100) having a data/control bus interface;

a data/control bus (104) implementing one or more device communication channels;

a mass storage device (118, 121 + 122) having an interface for communicating mass storage transactions;

a data memory (106) coupled to and shared by the processor and the mass storage device; and

a bus controller (102, or 114, or 102 and 114,) having a memory interface coupled to the data memory and a mass storage interface coupled to the mass storage device's interface and operable to conduct mass storage transactions without an intermediary mass storage controller (102 is directly coupled to 121+122 and 118 is directly coupled to 114) between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

wherein the mass storage device comprises:

a spinning disk having magnetic storage media provided on at least one surface;

a head for accessing data stored in the magnetic storage media;

an actuator mechanism for moving the head relative to the magnetic storage media in response to commands (col. 1, lines 37 – 52);

a servo controller coupled the data memory by the controller and configured to generate the commands to the actuator mechanism (figure 2).

6. With respect to claim 18, the mass storage device's interface is implemented by the servo controller and implements a physical interface to the data/control bus and a physical interface to the head and actuator mechanism (col. 5, lines 27 – 37).

7. Claims 7, 10 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunsakar, Zaiti, Moriarty, or Houston in view of Tanenbaum.

Each of the primary references discloses all of the limitations of claim 1 as discussed above. However, they do not specifically disclose that controller process and application behavior processes are implemented using the processor. Nor do they specifically disclose that the processor implements data structures storing physical geometry information about the mass storage devices. On the other hand, Tanenbaum discloses these (page 92, disk task, page 92, other task, for example, terminal, memory, clock, file system, and user programs, and pages 482 – 484).

It would have been obvious to one of ordinary skill in the art, having the teachings of each of the primary reference cited above and Tanenbaum before him at the time the invention was made, to use Tanenbaum's teachings in order to actually design and implement an operating system.

(10) Response to Argument

1. Rejection of Claims 1-3, 5, and 21 Under 35 U.S.C § 102 Based on Hunsaker is Proper

Applicant's characterization of Applicant's disclosed "computing system having **a bus controller with an interface** to both data memory and **a mass storage interface** without a mass storage controller" (Appeal Brief, page 5) is irrelevant and misleading. It is irrelevant because while the claim requires coupling the bus controller's mass storage interface with mass storage device's interface without an **intermediary** mass storage controller, it does not recite the limitation "a mass storage interface without a mass storage controller." It is misleading because Applicant's own figure 3 (see also specification, pages 11-12, paragraph 33) shows that the claimed mass storage interface is to the device's mass storage controller 303. The claimed mass storage device is simply a combination of a mass storage element and its controller.

As to Applicant's discussion of MCH 130 and ICH 150 shown in figure 1 of Hunsaker reference, Applicant seems to have misinterpreted the rejection. The rejection statement clearly identifies ICH 150, which provides control for various busses (e.g. PCI 160, interface bus to I/O devices 180, and other devices that connect to it), as the element that anticipates the claimed "bus controller having a memory interface ... and a mass storage interface ..." As clearly shown in Figure 1 of Hunsaker's disclosure, ICH 150 directly interfaces with the mass storage device 170 without an intermediary mass storage controller. ICH also has a separate interface (i.e. memory

interface) that connects directly to the memory controller hub 130 to couple to the system memory 140. The system memory 140 is only accessible through the memory controller 130. Any interaction with the system memory is through the memory controller 130. Therefore, interface to the memory controller is a memory interface.

Regarding Applicant's argument that the interface between ICH 150 and the memory controller 130 is a controller to controller interface, Applicant has not disclosed that the claimed bus controller provides memory control functions and acts as a memory controller. Nor has Applicant claimed a memory controller integrated into the claimed bus controller. One skilled in the art understands that raw storage devices are not directly accessible. They require controllers. Memory devices require controllers, to buffer and decode read/write commands and their associated addresses, to buffer data for reading/writing, and to supply timing and other control signals necessary to access data. An external interface to memory is an interface to its controller. If Applicant's system memory 411 is a new type of novel memory that does not require an interface through its controller for access, this novelty has not been disclosed or claimed. Hunsaker's system memory interface is through its memory controller 130. Applicant's failure to disclose the details of the system memory that shows that the interface to Applicant's system memory 411 is through its controller does not make Applicant's invention patentable.

As to Applicant's argument regarding there being no description of ICH 150 being configured to "conduct mass storage transactions between the data memory and the mass storage device", this issue has been addressed before in the Final Office Action mailed February 10,

2006. The limitation "conduct" has both active (to lead or to cause to act) and passive (to act as a medium or to provide channel) meanings. When Applicant asserted that prior art bus controllers do not teach the limitation "operable to conduct mass storage transactions ...", the Examiner interpreted this argument to mean that Applicant is attributing some kind of active role to the claimed bus controller in these transactions, because the prior art clearly teaches the claimed bus in its passive role, and asked for support for this argument. Applicant has not provided support for this argument and stated that Applicant was simply trying to stress that prior art does not teach each and every function called for in the claim (see After Final Amendment dated April 4, 2006, page 5). As far as the Examiner can discern, the claimed bus controller simply provides connection points or paths through which various system components communicate. There's no active role played by the bus controller to "conduct mass storage transactions." Moreover, even if Applicant can provide support for any active role that the bus controller may play, Applicant has not disclaimed the passive meaning of the limitation "conduct." As shown in figure 1, Hunsaker's ICH 150 provides connection points or paths between the memory system and the mass storage device 170. The Examiner also notes that the claimed bus controller is "operable" to conduct mass storage transactions. According to Merriam Webster's Collegiate Dictionary, 10th edition, "operable" means: fit, possible, or desirable to use. It is possible or desirable to use ICH 150 to conduct mass storage transactions between the memory 140 and the mass storage device 170 because it is the only means through which such transactions can be conducted. Moreover, Hunsaker specifically discloses, at page 2, paragraph 19, that the ICH 150 includes a Direct Memory Access (DMA) Controller and a mass

storage interface, among other interfaces. A DMA controller controls transactions between storage devices and memory without using processor resources.

As to Applicant's last argument, it is not clear to the Examiner what Applicant is trying to argue. Applicant seems to be arguing that the manner in which ICH 150 communicates with the mass storage device 170 is different from the manner in which the claimed bus controller communicates with the claimed mass storage device. However, the manner in which the bus controller communicates with the mass storage device is not claimed. The claim merely requires that the interface couple to the mass storage device's interface without an intermediary storage controller. There is no intermediary storage controller between ICH 150 and the mass storage device 170. Applicant also argues that there is no discussion of the "mass storage interface" called for in claim 1, because Hunsaker does not teach or suggest such a direct interface as required under 35 U.S.C 102. It is not clear to the Examiner what Applicant means by "such a direct interface", as no "direct interface" is claimed. Hunsaker clearly discloses a mass storage interface without an intermediary controller as claimed.

2. Rejection of Claims 1, 12, and 20 Under 35 U.S.C § 102 Based on Zaidi is Proper

Applicant seems to be arguing that because Zaidi teaches a "bridge" instead of a "bus controller", Zaidi fails to anticipate the instant claim even though the "bridge" meets all of the structural and functional limitations of the claimed "bus controller." Zaidi's "bridge" provides control and access to various buses as shown in figure 28. It also provides an interface to the

CPU to its left, an interface to the memory (DRAM) to its right and an interface to the PCI bus through which it interfaces with mass storage devices (DMA peripherals which Zaidi discloses to include mass storage devices, col. 27, lines 41-45). Applicant further argues that Zaidi does not disclose a data memory coupled to the processor as called for in claim 1, because the DRAM is couple to the memory bus (m-bus). Applicant is correct in that the DRAM is coupled to the memory bus. However, this does not mean that the memory is not coupled to the processor as Applicant contends. If the DRAM is not coupled to the processor, the system of Zaidi would be non-functional, as the processor would have no access to the memory. Applicant also asserts that Zaidi does not teach that its bridge is capable of conducting mass storage transactions between the data memory and the mass storage devices. Contrary to Applicant's assertion, as shown in the figure, the bridge is the only channel or medium through which transactions between a DMA peripheral can transfer data to the memory. Instead of disclosing a mere possibility of conducting such transactions through the bridge as claimed, Zaidi actually teaches such transactions. Zaidi discloses DMA peripherals that are mass storage devices. DMA is an acronym for Direct Memory Access. DMA is also a term of art. DMA peripherals have direct access to memory and transact with memory directly without involving the processor.

With respect to Applicant's assertion that the Examiner seems to be shifting the duty to show each and every limitation onto the Applicant, when the Examiner presents a prima facie case of anticipation by pointing out how each element is anticipated by the prior art reference as was done here, the burden of proof, that the applied reference does not anticipate, shifts to Applicant. To be successful, Applicant must point out which elements are not taught by the prior

art and discuss why the prior art elements pointed out in the rejection do not read on the claim language in a reasonable and convincing manner. Applicant has failed to do so in the past replies.

3. Rejection of Claims 1, 14, and 20 Under 35 U.S.C § 102 Based on Moriarty is Proper

Moriarty discloses, in figure 1, a host/PCI bus bridge that interfaces with the memory subsystem 104 on the host bus side and a mass storage device that comprises a controller 118 and a hard disk 144 on the PCI bus side. When broadly interpreted, the host bus interface reads on the claimed memory interface because the host bus provides direct interface between the bridge and the memory system. It is the only interface through which the system components on the PCI side can access the memory subsystem. The Examiner believes that this is a reasonable interpretation. The only claimed "feature" that is related to this interface is that it couples to the data memory. Moriarty's bridge directly couples to the memory via this interface. Likewise, the PCI side of the bride interfaces with the mass storage device (118 and 144 combination) without any other intermediary device. Therefore, the bridge's PCI interface reads on the claimed "mass storage interface." The Examiner can discern no patentable distinction between the mass storage device taught by Moriarty and the claimed mass storage device that consists of a controller 303 and a disk drive 307. As to Applicant's argument regarding multiple bus traversal required in the system of Moriarty vs. the invention of claim 1, bus traversals do not appear in the claims at all.

4. Rejection of Claims 1 and 19 Under 35 U.S.C § 102 Based on Ellison is Proper

Grounds of rejections based on Ellison are almost identical to those based on Hunsaker and the same arguments apply. Therefore, they will not be repeated here.

5. Rejection of Claims 17 and 18 Under 35 U.S.C § 102 Based on Houston is Proper

Applicant argued that claim 1 has never been rejected as being anticipated by Houston. Applicant is technically correct in that claim 1 has not been explicitly rejected with the Houston reference. On the other hand, rejection of claim 17, which includes all of the limitations of claim 1, is an implicit rejection of claim 1. The rejection of claim 17 shown above explicitly recites and shows how the limitations of claim 1 are met by Houston's disclosure.

Applicant argues that "[c]laim 1 calls for the bus controller to interface with a mass storage device without a mass storage controller but such an intermediary storage controller would be used with the HDs of Houston, e.g., see Figure 2, and controller 214." (Appeal Brief, page 13, first paragraph). Applicant is correct that Houston's HDs requires a disk controller as shown in figure 2. However, Applicant's HD (figure 3, 307) also requires a disk controller (303, see also specification, page 12, paragraph 33). Applicant seems to be claiming that the novelty of the invention lies in the way Applicant chooses to arbitrarily define what a mass storage device is. Here, Applicant seems to be arguing that Applicant's definition of a mass storage device as applied to Applicant's invention is a device that includes the drive mechanism (307) and its controller (303) and therefore, Applicant's mass storage device does not require a mass

storage controller, while Applicant's definition of a mass storage device as applied to the prior art device is the drive mechanism only without its controller and therefore, the prior art mass storage device requires a mass storage controller. Choosing to call the combination of a drive mechanism and a controller a mass storage device does not make it patentably distinct from the prior art combination of a drive mechanism and a controller regardless of how Applicant chooses to label them.

6. Rejection of Claims 7, 10, and 32 Under 35 U.S.C § 103 Based on Hunsaker, Zaidi, Moriatry, or Houston in view of Tanenbaum is Proper

Applicant's argument amounts to an allegation that Tanenbaum reference is not an anticipating disclosure. The Examiner has not asserted that Tanenbaum is an anticipating reference. Instead, the claims were rejected as being obvious over the references that anticipate claim 1 in view of Tanenbaum. Applicant has failed to make an effective argument regarding the combination of the references, and therefore, has not overcome the prima facie case of obviousness presented in the final rejection.

With respect to claim 32, the main difference between this claim and claim 1 is the "first mass storage device" limitation. The Examiner notes that each of the primary references shows more than one mass storage device (Hunsaker figure 1 and Ellison figure 1C, 172, 174, 176, and other PCI peripherals; Zaidi, two DMA peripherals shown in figure 28; Moriarty, figure 1, 138; Houston, figure 1, 122, 118, 134, 120) that is accessible to the processor. The claim merely requires that the first mass storage device be coupled to the data/control bus. It does not require

that the first mass storage device be **directly** coupled to the data/control bus. For example, the CD ROM 172 and its controller 170 of Hunsaker or any of the other PCI devices on the PCI buses are coupled to the data/control bus (host bus 120) and are accessible to the processor 110.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the reasons stated above, it is believed that the rejections should be sustained.

Respectfully submitted,

Woo H. Choi
Primary Patent Examiner
February 13, 2007

Conferees

Reginald Bragdon
Supervisory Patent Examiner
February 13, 2007

REGINALD BRAGDON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Lynne Browne
Appeal Practice Specialist, TQAS
February 13, 2007

Lynne H. Browne
Appeal Specialist, TQAS
Technology Center 2100

Kent A. Lembke
STMicroelectronics, Inc
1310 Electronics Drive
Carrollton, TX 75006